

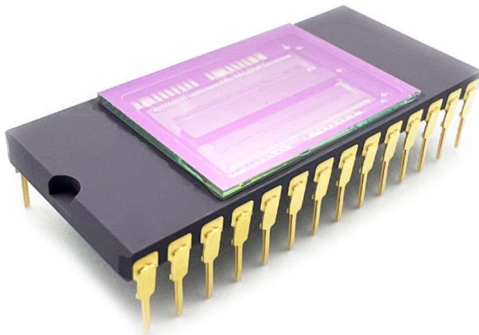
Near-Infrared Linear Image Sensor (0.9 – 1.7 μm) with 1024 x 1 pixels

FEATURES

- 1024 x 1 pixels
[pixel size: S 12.5 x 12.5, M 12.5 x 250 μm]
- 28-pin Ceramic DIP (CDIP)
- Built-in Temperature Sensor
- 0.9 μm – 1.7 μm Spectral Range
- Minimum Pixel Operability > 99%
- Quantum Efficiency > 70%
- Snapshot ITR / IWR
- 2 Outputs with up to 22 MHz Pixel Rate

APPLICATIONS

- Shortwave-Infrared Imaging
- Semiconductor Inspection / Process Monitoring
- Sorting / Recycling
- Near-Infrared Spectrophotometry



The LDA1024 is an uncooled near-infrared linear image sensor consisting of a linear InGaAs-detector array bonded to the p-on-n readout-IC. The series contains two products with different sensor pixel sizes. LDA512P25S-17-C, and LDA512P25M-17-C.

GENERAL DESCRIPTIONS

Parameter	Unit	Value	
Sensor Technology	---	Planar InGaAs PIN	
Spectral Range	μm	0.9 – 1.7	
Actual Pixel Array	---	1024 x 1	
Pixel Pitch	μm	12.5	
Pixel Size	μm	Pixel Size	Dimension
		S	12.5 x 12.5
		M	12.5 x 250
Chip Size	mm	15.3 x 9.0	

Package Type	---	28-pin Ceramic DIP (CDIP)
Package Size L x W x T	mm	35.56 x 15.61 x 7.15
Weight	g	5.18

SPECIFICATIONS (¹ITS = 20 ± 1°C)

Parameter	Unit	Value	Conditions
^{2,3} Dark Current	fA	S ≤ 600	Photo pixel biased @ -0.5 V
		M ≤ 1000	
² Quantum Efficiency * Fill Factor (QE _{EFF})	%	≥ 70	λ = 1550 nm
² Response Nonuniformity	%	≤ 5	At 50% Full Well
² Response Nonlinearity	%	≤ 2	15% – 85% Well Occupation Range
Charge Capacity	μV/e-	C _{int} = 6.4 fF	16 settings from 6.4 fF to 2.1 pF
		C _{int} = 16 fF	
		C _{int} = 30 fF	
		C _{int} = 120 fF	
		C _{int} = 2.1 pF	
Readout Noise	mV	C _{int} = 6.4 fF	ROIC Specifications
		C _{int} = 16 fF	
		C _{int} = 30 fF	
		C _{int} = 120 fF	
		C _{int} = 2.1 pF	
Output Swing	V	≥ 2.0	Gain @ 16 fF (High Gain Mode)
Minimum Integration Period	μs	5	ROIC Specifications
Maximum Pixel Rate	MHz	22	ROIC Specifications
² Pixel Operability	%	≥ 99	Percentage of Pixels with QE _{EFF} Deviation within ± 20%*(QE _{EFF} Mean)

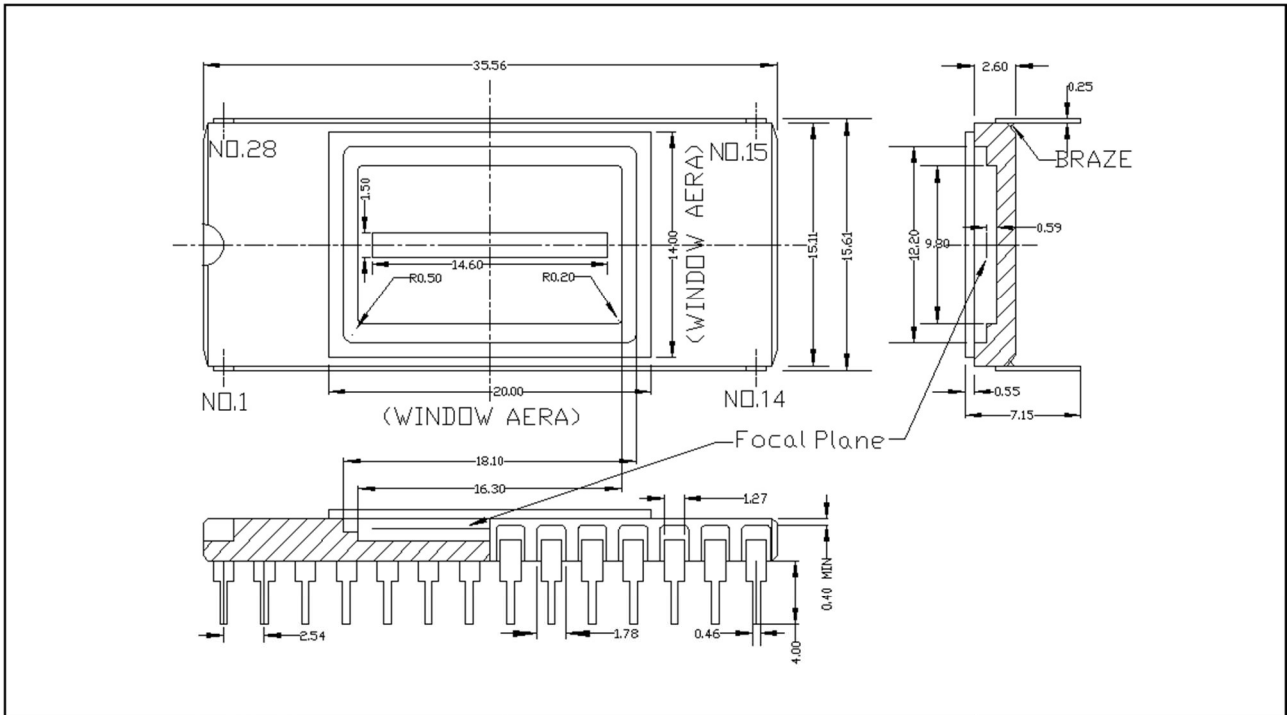
1. Readings from Integrated Temperature Sensor (ITS).
2. These items are defined for central effective pixel array (1024x1). Their values correspond to default operation conditions.
3. High gain, charge capacity @16fF, integration time 5ms.

ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Min.	Max.
⁴ Operating Temperature	°C	-40	+70
⁴ Storage Temperature	°C	-40	+70
⁵ Power Consumption	mW	---	190

4. In non-condensing environment.
5. Without powering on the thermoelectric cooler.

PACKAGE OUTLINE (Unit: mm)

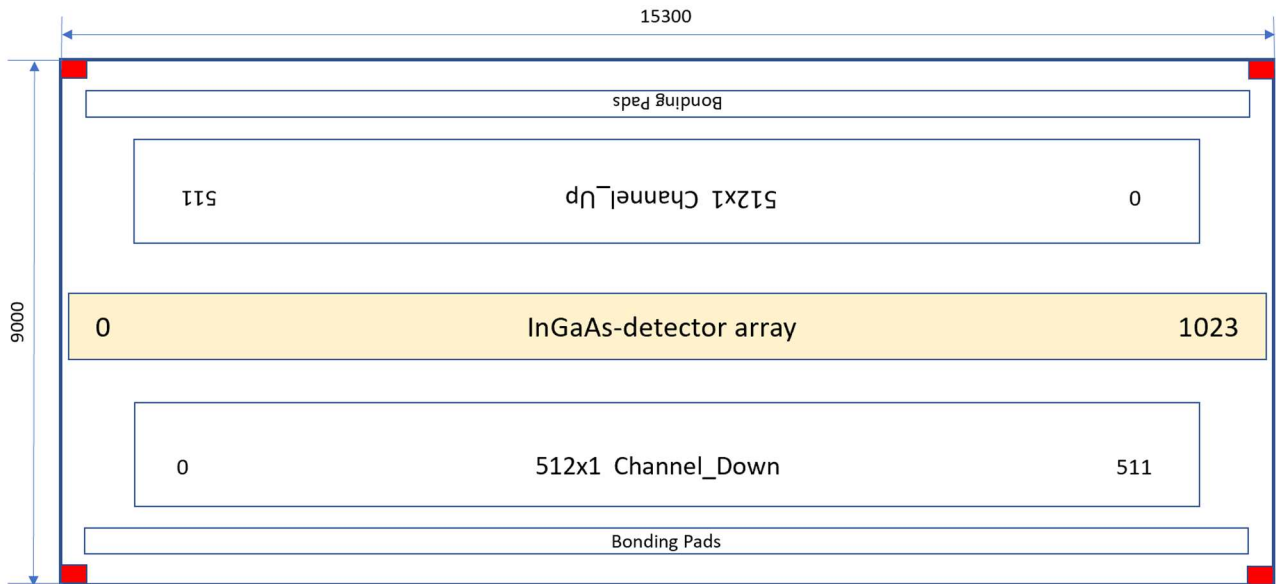


PIN DEFINITION								 InGaAs linear Image Sensor 1024 x 1		
01	VDD_D	08	SDOUT_D	15	GND	22	SDIN_U			
02	RESET_D	09	DATVALID_D	16	VR1_U	23	CEB_U			
03	NC	10	VOUT_D	17	VR2_U	24	MC_U	Chunghwa Leading Photonics Tech Co.,Ltd All right reserved		
04	INT_D	11	VDDA_D	18	VTEMP_U	25	INT_U			
05	MC_D	12	VR2_D	19	VDDA_U	26	NC	UNIT:mm	Edition:1.2	2023.1.11
06	CEB_D	13	VR1_D	20	VOUT_U	27	RESET_U			
07	SDIN_D	14	VDETCOM	21	SDOUT_U	28	VDD_U			

Pin Definition							
01	VDD_D	08	SDOUT_D	15	GND	22	SDIN_U
02	RESET_D	09	DATVALID_D	16	VR1_U	23	CEB_U
03	NC	10	VOUT_D	17	VR2_U	24	MC_U
04	INT_D	11	VDDA_D	18	VTEMP_U	25	INT_U
05	MC_D	12	VR2_D	19	VDDA_U	26	NC
06	CEB_D	13	VR1_D	20	VOUT_U	27	RESET_U
07	SDIN_D	14	VDETCOM	21	SDOUT_U	28	VDD_U

CHIP PROFILE

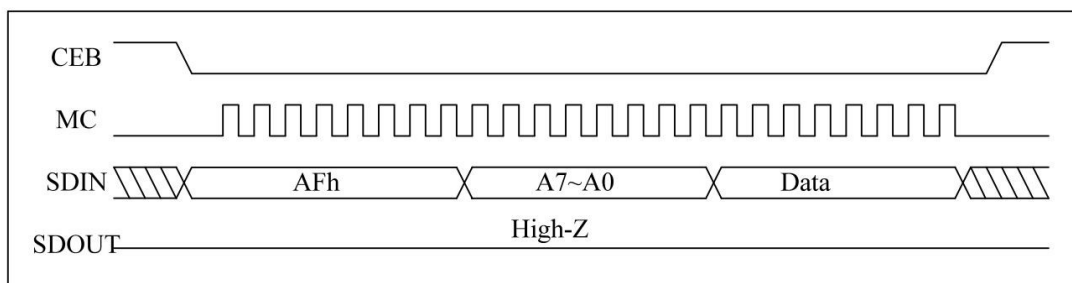
Layout



Chip size:15.3mm x 9.0mm

SPI Interface

LDA1024 supports SPI protocol to set the command registers. There are functions of the gain mode, power consumption control and the sequence of pixel output. The 1024x1 photodiode array is connected to two 512x1 readout ICs.



SPI Protocol Schematic

OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
01, 28	VDD_D, VDD_U	1.8 V	> 30 mA	Positive logic supply
11, 19	VDDA_D, VDDA_U	3.6 V	> 60 mA	Positive analog supply
12, 17	VR2_D, VR2_U	0.3 V	> 30 mA	External Input Bias
13, 16	VR1_D, VR1_U	2.3 V	> 5 mA	External Input Bias
14	VDETCOM	> VR1_D&U	--	Detector common voltage ⁶ Detector bias = VDETCOM - VR1_D&U
15	GND	0 V	--	Ground
02, 27	RESET_D, RESET_U	1.8 V	--	Chip reset

6. VDETCOM lower than 2.3 V will forward bias the sensor, the exact zero bias voltage is device and temperature dependent.

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
04, 25	INT_D, INT_U	1.8 V / 0 V	< 50 nS	Integration time
05, 24	MC_D, MC_U	1.8 V / 0 V	< 5 nS	Master clock Max. Freq. = 22 MHz
06, 23	CEB_D, CEB_U	1.8 V / 0 V	< 10 nS	⁷ Chip enable
07, 22	SDIN_D, SDIN_U	1.8 V / 0 V	< 5 nS	Data code input

7. The input and output of all commands start after the falling edge of CEB.

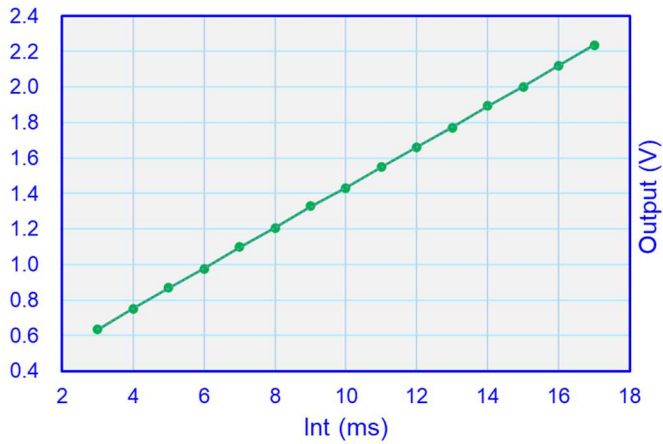
Digital Pattern Output

Pin #	Clocks	Levels	Rise/Fall	Remark
08, 21	SDOUT_D, SDOUT_U	1.8V/0V	--	Data code output
09	DATVALID_D	1.8V/0V	--	Valid data output flag signal

Analog Output

Pin #	Outputs	Levels	Value	Remark
10, 20	VOOUT_D, VOOUT_U	0.2 ~ 2.4 V	--	Video output
18	VTEMP_U	2.138 V	27°C	Integrated Temperature Sensor (-0.6 mV / °C)

Output Linearity



Measurement Conditions	
Illumination	1550 nm
Gain	@16 fF
Integration Time	15 ~ 85% Well Occupation
	3 ms ~ 17 ms
ITS	20 \pm 1 $^{\circ}$ C
Detector Bias	Vdetcom = 2.8 V (bias = -0.5 V)
Outputs	2 output mode
Screen Size	1024 x 1

QEFF Spectrum (typical example)

