

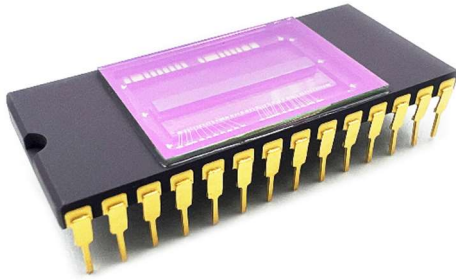
Near-Infrared Linear Image Sensor (0.9 – 1.7 μm) with 512 x 1 pixels

FEATURES

- 512 x 1 pixels
[pixel size: S 25 x 25, M 25 x 250, L 25 x 500 μm]
- 28-pin Ceramic DIP (CDIP)
- Built-in Temperature Sensor
- 0.9 μm – 1.7 μm Spectral Range
- Minimum Pixel Operability > 99%
- Quantum Efficiency > 70%
- Snapshot ITR / IWR
- One output with up to 22 MHz Pixel Rate

APPLICATIONS

- Shortwave-Infrared Imaging
- Semiconductor Inspection / Process Monitoring
- Sorting / Recycling
- Near-Infrared Spectrophotometry



The LDA512-C series is an uncooled near-infrared linear image sensor consisting of a linear InGaAs-detector array bonded on the p-on-n readout-IC. The series contains three products with different sensor pixel sizes. LDA512P25S-17-C, LDA512P25M-17-C, LDA512P25L-17-C.

GENERAL DESCRIPTIONS

Parameter	Unit	Value	
Sensor Technology	---	Planar InGaAs PIN	
Spectral Range	μm	0.9 – 1.7	
Actual Pixel Array	---	512 x 1	
Pixel Pitch	μm	25	
Pixel Size	μm	Pixel Size	Dimension
		S	25 x 25
		M	25 x 250
		L	25 x 500
Chip Size	mm	15.3 x 4.5	

Package Type	---	28-pin Ceramic DIP (CDIP)
Package Size L x W x T	mm	35.56 x 15.61 x 7.15
Weight	g	5.09

SPECIFICATIONS (¹ITS = 20 ± 1°C)

Parameter		Unit	Value	Conditions
^{2,3} Dark Current		fA	S ≤ 400	Photo pixel biased @ -0.5 V
			M ≤ 600	
			L ≤ 1000	
² Quantum Efficiency * Fill Factor (QE _{EFF})		%	≥ 70	λ = 1550 nm
² Response Nonuniformity		%	≤ 5	At 50% Full Well
² Response Nonlinearity		%	≤ 2	15% – 85% Well Occupation Range
Charge Capacity	C _{int} = 6.4 fF	μV/e ⁻	25	16 settings from 6.4 fF to 2.1 pF
	C _{int} = 16 fF		10	
	C _{int} = 30 fF		5.3	
	C _{int} = 120 fF		1.3	
	C _{int} = 2.1 pF		0.076	
Readout Noise	C _{int} = 6.4 fF	mV	1.2	ROIC Specifications
	C _{int} = 16 fF		0.8	
	C _{int} = 30 fF		0.6	
	C _{int} = 120 fF		0.5	
	C _{int} = 2.1 pF		0.25	
Output Swing		V	≥ 2.0	Gain @ 120 fF
Minimum Integration Period		μs	5	ROIC Specifications
Maximum Pixel Rate		MHz	22	ROIC Specifications
² Pixel Operability		%	≥ 99	Percentage of Pixels with QE _{EFF} Deviation within ± 20% *(QE _{EFF} Mean)

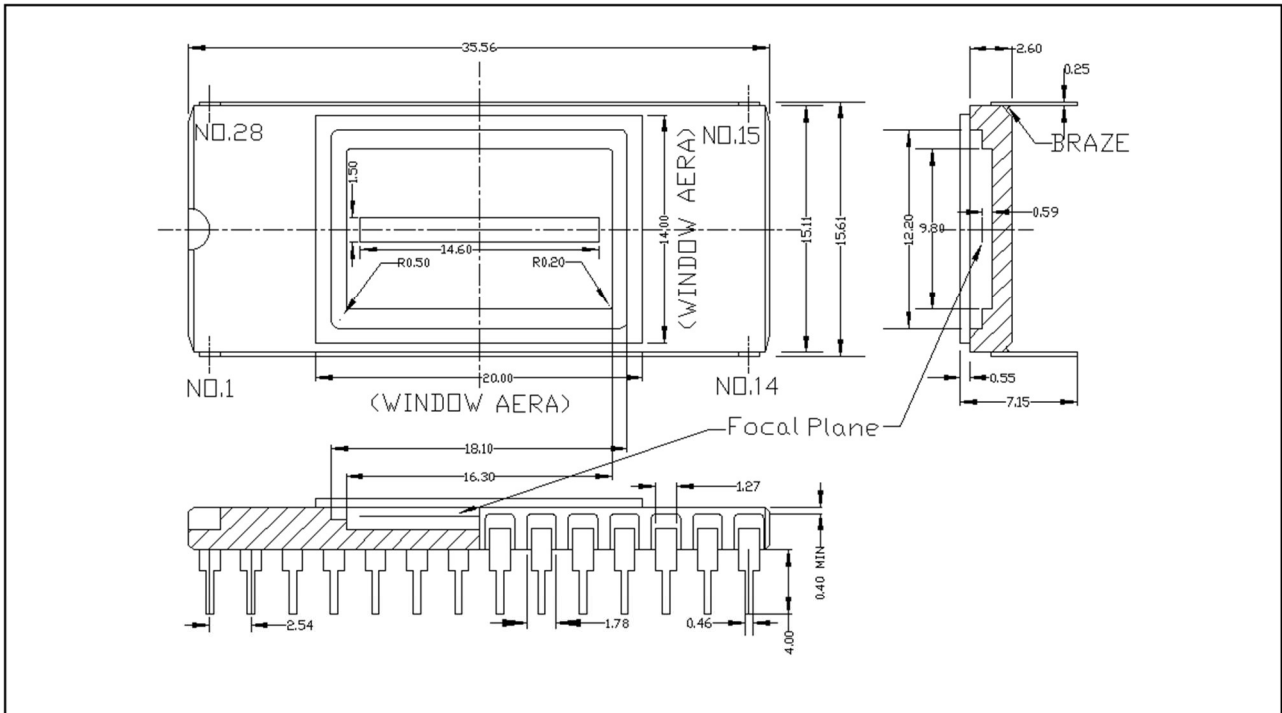
- Readings from Integrated Temperature Sensor (ITS).
- These items are defined for central effective pixel array (512x1). Their values correspond to default operation conditions.
- Medium gain, charge capacity @120fF, integration time 5ms.

ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Min.	Max.
⁴ Operating Temperature	°C	-40	+70
⁴ Storage Temperature	°C	-40	+70
⁵ Power Consumption	mW	---	95

- In non-condensing environment.
- Without powering on the thermoelectric cooler.

PACKAGE OUTLINE (Unit: mm)

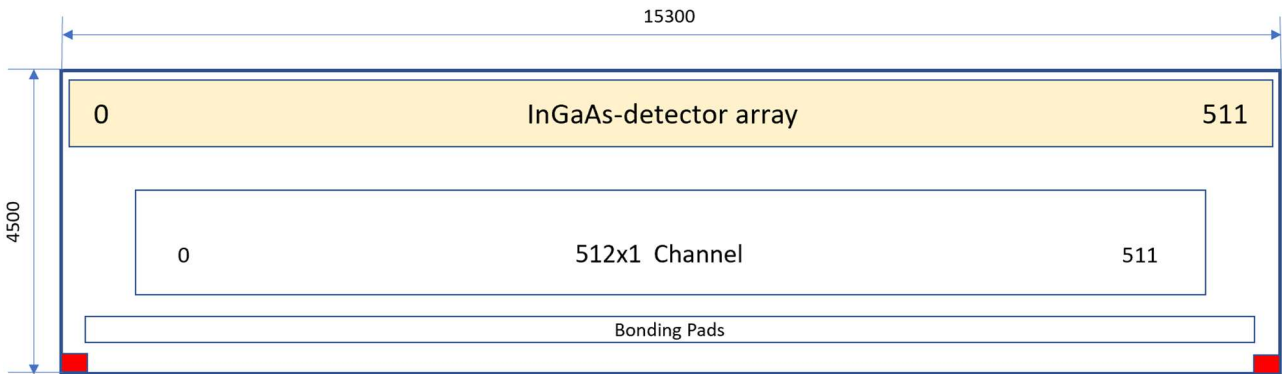


PIN DEFINITION							InGaAs linear Image Sensor 512 x 1		
01	VDD	08	SDOUT	15	GND		22	NC	Package Type : 28-pin Ceramic DIP UNIT:mm Edition:1.2 2023.1.11
02	RESET	09	DATVALID	16	NC	23	NC		
03	NC	10	VOUT	17	NC	24	NC		
04	INT	11	VDDA	18	TEMP	25	NC		
05	MC	12	VR2	19	NC	26	NC		
06	CEB	13	VR1	20	NC	27	NC		
07	SDIN	14	VDETCOM	21	NC	28	NC		
						Chunghwa Leading Photonics Tech Co.,Ltd All right reserved			

PIN DEFINITION							
01	VDD	08	SDOUT	15	GND	22	NC
02	RESET	09	DATVALID	16	NC	23	NC
03	NC	10	VOUT	17	NC	24	NC
04	INT	11	VDDA	18	VTEMP	25	NC
05	MC	12	VR2	19	NC	26	NC
06	CEB	13	VR1	20	NC	27	NC
07	SDIN	14	VDETCOM	21	NC	28	NC

CHIP PROFILE

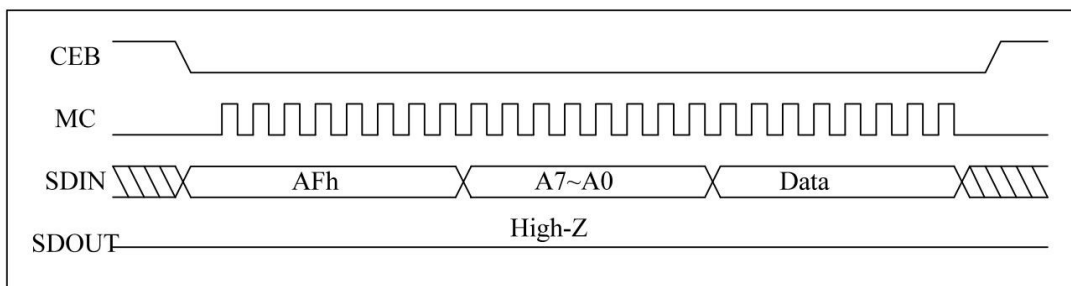
Layout



Chip size:15.3mm x 4.5mm

SPI Interface

LDA512 supports SPI protocol to set the command registers. There are functions of the gain mode, power consumption control and the sequence of pixel output.



SPI Protocol Schematic

OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
01	VDD	1.8 V	> 30 mA	Positive logic supply
11	VDDA	3.6 V	> 60 mA	Positive analog supply
12	VR2	0.3 V	> 30 mA	External Input Bias
13	VR1	2.3 V	> 5 mA	External Input Bias
14	VDETCOM	> VR1	--	Detector common voltage ⁶ Detector bias = VDETCOM - VR1
15	GND	0 V	--	Ground
02	RESET	1.8 V	--	Chip reset

6. VDETCOM lower than 2.3 V will forward bias the sensor, the exact zero bias voltage is device and temperature dependent.

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
04	INT	1.8 V / 0 V	< 50 nS	Integration time
05	MC	1.8 V / 0 V	< 5 nS	Master clock Max. Freq. = 22 MHz
06	CEB	1.8 V / 0 V	< 10 nS	⁷ Chip enable
07	SDIN	1.8 V / 0 V	< 5 nS	Data code input

7. The input and output of all commands start after the falling edge of CEB.

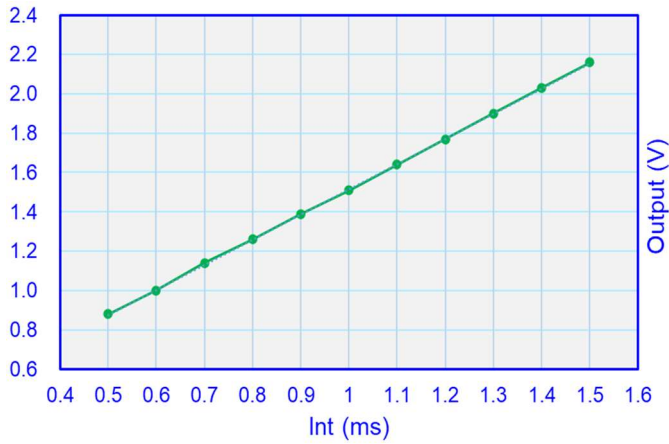
Digital Pattern Output

Pin #	Clocks	Levels	Rise/Fall	Remark
08	SDOUT	1.8 V / 0 V	--	Data code output
09	DATVALID	1.8 V / 0 V	--	Valid data output flag signal

Analog Output

Pin #	Outputs	Levels	Value	Remark
10	VOUT	0.2 ~ 2.4 V	--	Video output
18	VTEMP	2.138 V	27°C	Integrated Temperature Sensor (-0.6 mV / °C)

Output Linearity



Measurement Conditions	
Illumination	1550 nm
Gain	@120 fF
Integration Time	15 ~ 85% Well Occupation
	0.5 ms ~ 1.4 ms
ITS	20 \pm 1 $^{\circ}$ C
Detector Bias	Vdetcom = 2.8 V (bias = -0.5 V)
Screen Size	512 x 1

QEFF Spectrum (typical example)

