Near-Infrared Linear Image Sensor (0.9 – 1.7 µm) with 1024 x 1 pixels

FEATURES

- 1024 x 1 pixels
  [pixel size: S 12.5 x 12.5, M 12.5 x 250 µm]
- 28-pin Metal DIP Package
- Embedded Thermoelectric Cooler
- Built-in Temperature Sensor
- 0.9 µm – 1.7 µm Spectral Range
- Minimum Pixel Operability > 99%
- Quantum Efficiency > 70%
- Snapshot ITR / IWR
- 2 Outputs with up to 22 MHz Pixel Rate

APPLICATIONS

- Shortwave-Infrared Imaging
- Hyper- / Multi-Spectral Imaging
- Semiconductor Inspection / Process Monitoring
- Sorting / Recycling

The LDA1024 is a near-infrared linear image sensor consisting of a linear InGaAs-detector array bonded to the p-on-n readout-IC. The series contains two products with different sensor pixel sizes. LDA512P25S-17-T1, and LDA512P25M-17-T1.

GENERAL DESCRIPTIONS

Parameter	Unit	Value	
Sensor Technology	---	Planar InGaAs PIN	
Spectral Range	µm	0.9 – 1.7	
Actual Pixel Array	---	1024 x 1	
Pixel Pitch	µm	12.5	
Pixel Size	µm	Pixel Size	Dimension
		S	12.5 x 12.5
		M	12.5 x 250
Chip Size	mm	15.3 x 9.0	

Package Type	---	28-pin Metal DIP Package
Package Size L x W x T	mm	50.00 x 25.40 x 11.67
Weight	g	25.9

SPECIFICATIONS ([1]ITS = 20 ± 1℃)

Parameter		Unit	Typical Value		Conditions
[2,3]Dark Current		fA	S	≤ 600	Photo pixel biased @ -0.5 V
			M	≤ 1000	
[2]Quantum Efficiency * Fill Factor (QEFF)		%	≥ 70		λ = 1550 nm
[2]Response Nonuniformity		%	≤ 5		At 50 % Full Well
[2]Response Nonlinearity		%	≤ 2		15 % – 85 % Well Occupation Range
Charge Capacity	Cint = 6.4 fF	μV/e-	25		16 settings from 6.4 fF to 2.1 pF
	Cint = 16 fF		10		
	Cint = 30 fF		5.3		
	Cint = 120 fF		1.3		
	Cint = 2.1 pF		0.076		
Readout Noise	Cint = 6.4 fF	mV	1.2		ROIC Specifications
	Cint =16 fF		0.8		
	Cint = 30 fF		0.6		
	Cint = 120 fF		0.5		
	Cint = 2.1 pF		0.25		
Output Swing		V	≥ 2.0		Gain @16 fF (High Gain Mode)
Minimum Integration Period		μs	5		ROIC Specifications
Maximum Pixel Rate		MHz	22		ROIC Specifications
[2]Pixel Operability		%	≥ 99		Percentage of Pixels with QEFF Deviation within ± 20%*(QEFF Mean)

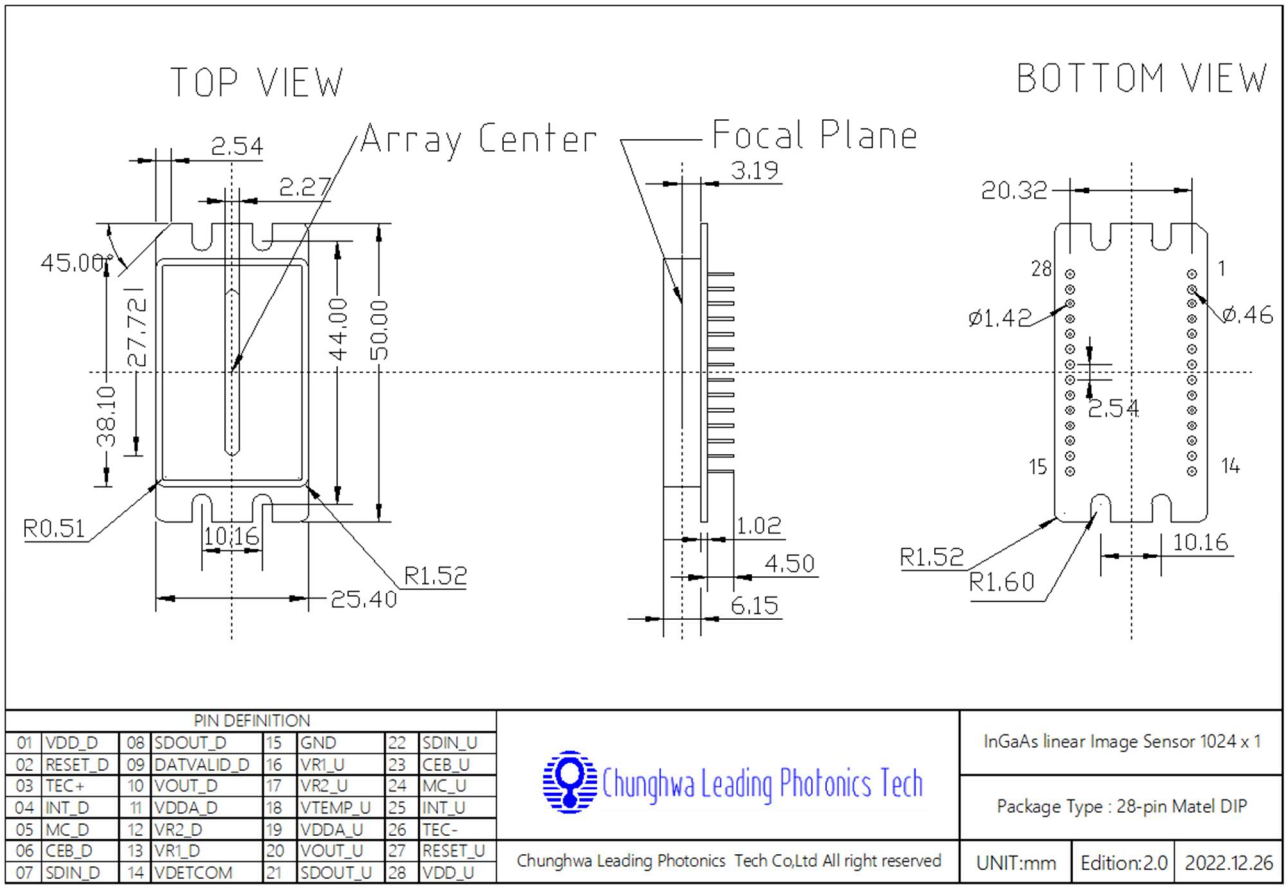
1. Readings from Integrated Temperature Sensor (ITS).
2. These items are defined for central effective pixel array (1024x1). Their values correspond to default operation conditions.
3. High gain, charge capacity @16fF, integration time 5ms.

ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Min.	Max.
[4]Operating Temperature	℃	-40	+70
[4]Storage Temperature	℃	-40	+70
[5]Power Consumption	mW	---	190

4. In non-condensing environment.
5. Without powering on the thermoelectric cooler.

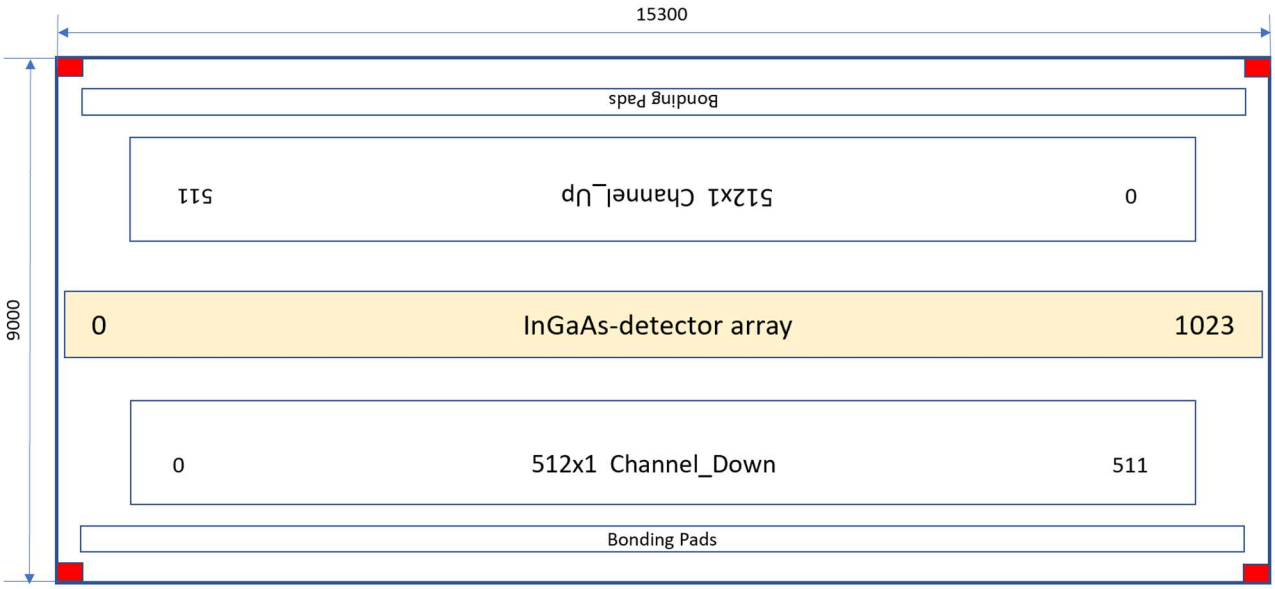
PACKAGE OUTLINE (Unit: mm)



Pin Definition							
01	VDD_D	08	SDOUT_D	15	GND	22	SDIN_U
02	RESET_D	09	DATVALID_D	16	VR1_U	23	CEB_U
03	TEC+	10	VOUT_D	17	VR2_U	24	MC_U
04	INT_D	11	VDDA_D	18	VTEMP_U	25	INT_U
05	MC_D	12	VR2_D	19	VDDA_U	26	TEC-
06	CEB_D	13	VR1_D	20	VOUT_U	27	RESET_U
07	SDIN_D	14	VDETCOM	21	SDOUT_U	28	VDD_U

CHIP PROFILE

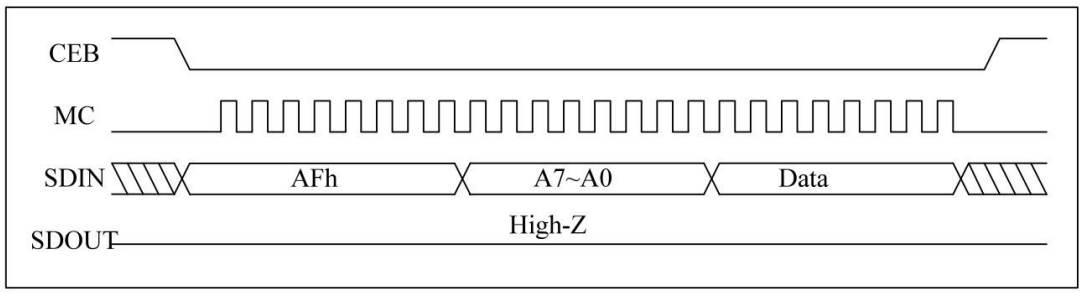
Layout



Chip size:15.3mm x 9.0mm

SPI Interface

LDA1024 supports SPI protocol to set the command registers. There are functions of the gain mode, power consumption control and the sequence of pixel output. The 1024x1 photodiode array is connected to two 512x1 readout ICs.



SPI Protocol Schematic

OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
01, 28	VDD_D, VDD_U	1.8 V	> 30 mA	Positive logic supply
11, 19	VDDA_D, VDDA_U	3.6 V	> 60 mA	Positive analog supply
12, 17	VR2_D, VR2_U	0.3 V	> 30 mA	External Input Bias
13, 16	VR1_D, VR1_U	2.3 V	> 5 mA	External Input Bias
14	VDETCOM	> VR1_D&U	--	Detector common voltage [6]Detector bias = VDETCOM - VR1_D&U
15	GND	0V	--	Ground
03	TEC+	0 V ~ 5.3 V	< 2.2 A	Positive TEC supply
26	TEC-	0 V	--	TEC ground
02, 27	RESET_D, RESET_U	1.8 V	--	Chip reset

6. VDETCOM lower than 2.3 V will forward bias the sensor, the exact zero bias voltage is device and temperature dependent.

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
04, 25	INT_D, INT_U	1.8 V / 0 V	< 50 nS	Integration time
05, 24	MC_D, MC_U	1.8 V / 0 V	< 5 nS	Master clock Max. Freq. = 22 MHz
06, 23	CEB_D, CEB_U	1.8 V / 0 V	< 10 nS	[7]Chip enable
07, 22	SDIN_D, SDIN_U	1.8 V / 0 V	< 5 nS	Data code input

7. The input and output of all commands start after the falling edge of CEB.

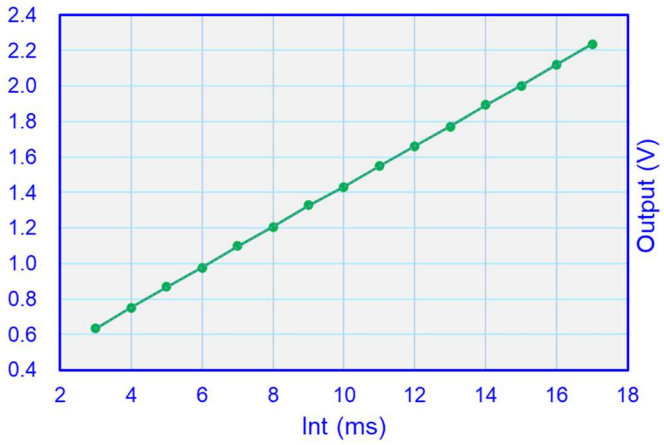
Digital Pattern Output

Pin #	Clocks	Levels	Rise/Fall	Remark
08, 21	SDOUT_D, SDOUT_U	1.8 V / 0 V	--	Data code output
09	DATVALID_D	1.8 V / 0 V	--	Valid data output flag signal

Analog Output

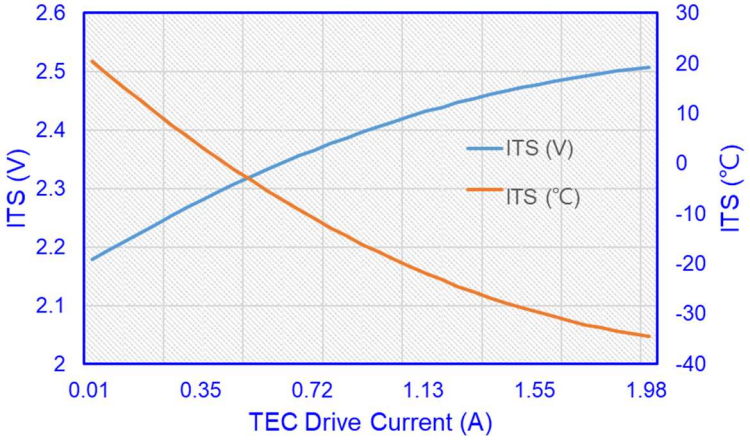
Pin #	Outputs	Levels	Value	Remark
10, 20	VOUT_D, VOUT_U	0.2 ~ 2.4 V	--	Video output
18	VTEMP_U	2.138 V	27℃	Integrated Temperature Sensor (-0.6 mV /℃)

Output Linearity



Measurement Conditions	
Illumination	1550 nm
Gain	@16 fF
Integration Time	15 ~ 85% Well Occupation
	3 ms ~ 17 ms
ITS	20 ± 1℃
Detector Bias	Vdetcom = 2.8 V (bias = -0.5 V)
Outputs	2 output mode
Screen Size	1024 x 1

Cooling Performance



QEFF Spectrum (typical example)